AMENDMENT TO THE CLAIMS

In the Claims

Please **ADD** new claims 33 and 34.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-7 (Canceled).

8. (Previously Presented) A method of enhancing stress in a semiconductor device, comprising:

depositing a layer of nitride film over a gate stack and a surface of a substrate; and

removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack,

wherein a gate is about 60 nm wide, a spacer is about 50 nm wide, and the nitride film provides a stress of about 2.0 GPa, the enhanced stress in the transistor channel is greater than approximately 4.5×10^9 dynes/cm^2 at about 5 nm below a gate oxide.

9. (Original) The method of claim 8, further comprising depositing a resist material on a surface of the nitride film over the substrate while leaving a surface of the nitride film proximate an upper portion of the gate stack exposed.

10. (Original) The method of claim 9, further comprising removing an upper portion of the gate stack and the nitride film disposed thereon.

11. (Previously Presented) The method of claim 9, wherein the depositing of the resist material comprises depositing one of a spin-on material, an anti-reflection coating, an oxide film, and a low k material.

12. (Original) The method of claim 11, further comprising forming spacers at a lower portion of the sidewalls of the gate stack.

13. (Previously Presented) The method of claim 12, wherein the forming of the spacers includes forming the spacers along substantially all of the sidewall and etching the spacers to form spacers at the lower portion of the sidewalls.

14. (Previously Presented) The method of claim 9, wherein the depositing of the resist material comprises depositing at least one of an oxide layer or a borophosphorosilicate glass on low spots and leaving high spots exposed.

15. (Previously Presented) The method of claim 10, wherein the removing of the upper portion of the gate stack and the nitride film disposed thereon comprises reactive ion etching.

16. (Previously Presented) The method of claim 10, wherein the removing of the upper portion of the gate stack and the nitride film disposed thereon comprises chemical mechanical polishing.

17. (Previously Presented) A method of enhancing stress in a semiconductor device, comprising:

depositing a layer of nitride film over a gate stack and a surface of a substrate;

removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack;

forming a spacer adjacent a sidewall of the gate stack; and

etching upper portions of the spacer to form sidewalls only at a lower portion of the gate stack.

Claim 18. (Canceled).

19. (Previously Presented) A method of enhancing stress in a semiconductor device, comprising:

depositing a layer of nitride film over a gate stack and a surface of a substrate; and

removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack,

wherein for a semiconductor device having a gate about 60 nm wide, a spacer about 50 nm wide, and a nitride film stress of about 2.0 GPa, the enhanced stress in the transistor channel is greater than approximately 5.5 x 10^9 dynes/cm^2 at about 5 nm below a gate oxide.

Claims 20-24 (Canceled).

25. (Previously Presented) The method of claim 19, further comprising depositing a resist material on a surface of the nitride film over the substrate while leaving a surface of the nitride film proximate an upper portion of the gate stack exposed.

26. (Previously Presented) The method of claim 19, further comprising removing an upper portion of the gate stack and the nitride film disposed thereon.

27. (Previously Presented) The method of claim 19, wherein the depositing of the resist material comprises depositing one of a spin-on material, an anti-reflection coating, an oxide film, and a low k material.

28. (Previously Presented) The method of claim 19, further comprising forming spacers at a lower portion of the sidewalls of the gate stack.

29. (Previously Presented) The method of claim 28, wherein the forming of the spacers includes forming the spacers along substantially all of the sidewall and etching the spacers to form spacers at the lower portion of the sidewalls.

30. (Previously Presented) The method of claim 19, wherein the depositing of the resist material comprises depositing at least one of an oxide layer or a borophosphorosilicate glass on low spots and leaving high spots exposed.

31. (Previously Presented) The method of claim 26, wherein the removing of the upper portion of the gate stack and the nitride film disposed thereon comprises reactive ion etching.

32. (Previously Presented) The method of claim 26, wherein the removing of the upper portion of the gate stack and the nitride film disposed thereon comprises chemical mechanical polishing.

33. (New) The method of claim 8, further comprising depositing a salicide gate region on top of the gate stack.

34. (New) The method of claim 8, wherein the substrate remains covered by the nitride film after the nitride film is removed from an upper portion of the gate stack.